

# Monolithic 100% Silicon Wafer Anode for All-Solid-State Batteries Achieving High Areal Capacity at Room Temperature

Ikcheon Na, Hwiho Kim, Sebastian Kunze, Chihyun Nam, Sugeun Jo, Hanbi Choi, Sumin Oh, Eugene Choi, Yong Bae Song, Yoon Seok Jung, Yun Seog Lee, and Jongwoo Lim\*



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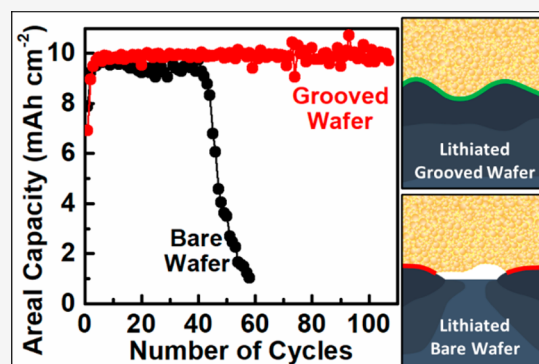


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Supporting Information

**ABSTRACT:** Silicon is an attractive anode material for all-solid-state batteries (ASSBs) because it has a high energy density and is safer than metallic lithium. Conventional silicon powder composite electrodes have significant internal voids and detrimental interfaces that suppress the lithium transport and lifetime. Here, we demonstrate that surface-treated thin silicon wafers could serve as monolithic additive-free, electrolyte-free, and void-free electrodes that can achieve high areal capacity at room temperature ( $\sim 25^\circ\text{C}$ ). A dense solid electrolyte interface could effectively suppress the cracks and pulverization found in the liquid electrolyte. We demonstrated that the grooved  $\langle 110 \rangle$  wafer exhibited reversible (de)lithiation owing to fast lithium distribution along the  $\langle 110 \rangle$  thickness direction. The surface groove could effectively penetrate the electrolyte layer, yielding a stable interfacial resistance and homogeneous alloying/dealloying processes during cycling. Our silicon wafer electrode achieved an areal capacity of  $10\text{ mAh cm}^{-2}$  at room temperature, which can be improved by further optimization.



The recent development of portable devices, electric vehicles, and large-scale energy storage systems has significantly increased the demand for safer and more energy-dense batteries.<sup>1–4</sup> All-solid-state batteries (ASSBs) utilizing sulfide-based electrolytes provide an ideal geometry to attain a higher energy density and improved safety compared with conventional lithium-ion batteries (LIBs) using flammable organic liquid electrolytes.<sup>5–7</sup>

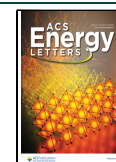
Silicon anodes exhibit a high specific capacity ( $3589\text{ mAh g}^{-1}$ ) via an alloy reaction, which is 10 times larger than that of graphite anodes ( $372\text{ mAh g}^{-1}$ ).<sup>8</sup> Because silicon is the second most abundant element in the Earth's crust, it is inexpensive and environmentally friendly.<sup>9</sup> Recent developments in metallic lithium anodes demonstrate impressive battery performance owing to their high specific capacity ( $3860\text{ mAh g}^{-1}$ ); however, they still face the risk of growing lithium dendrites and forming unstable solid electrolyte interfaces originating from the low reduction potential and high reactivity of lithium.<sup>10–14</sup> Moreover, room-temperature operation remains a challenge because the critical current density for reversible lithium metal deposition/depletion is still low.<sup>15</sup> Therefore, a silicon anode could be an attractive choice as a safer electrode with a high energy density.

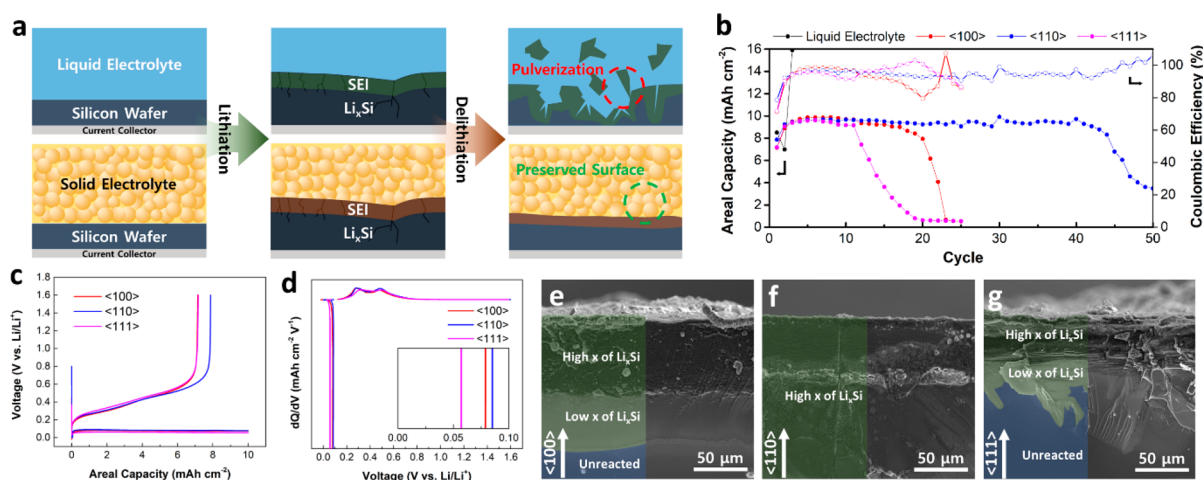
In several previous studies, silicon powder composite electrodes were developed as anodes for ASSBs.<sup>16–18</sup> Such silicon powders are generally mixed with electrolyte powders, carbon additives, and polymeric binders forming 3-dimensionally percolated interfaces in composite electrodes. Having large interface areas is not ideal because a detrimental solid-electrolyte-interphase (SEI) grown from the interfaces could decrease the lithium transport and capacity.<sup>19</sup> Because carbon additives are reactive to sulfide electrolytes, silicon powder electrodes with neither carbon species nor electrolytes have been demonstrated recently.<sup>20</sup> However, powder electrodes intrinsically have porous structures with many internal voids, even under a high fabrication pressure, which may impede lithium diffusion.<sup>21,22</sup> This remains a challenge in the fabrication of thick powder electrodes with a high areal

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**Figure 1.** Cell performance of silicon wafers for ASSBs. (a) Respective schematic illustrations of wafers under liquid and solid electrolyte system. (b) Cycling performance of wafers with liquid electrolyte and solid electrolyte at a current density of  $0.5 \text{ mA cm}^{-2}$ . (c) Voltage profiles, (d) differential capacity plots (inset is  $dQ/dV$  plots in voltage range of 0–0.1 V), and (e–g) cross-sectional SEM images of first lithiated bare <100>, <110>, and <111> wafers for ASSBs.

capacity. Thus, it is necessary to develop a new electrode design that can achieve a high areal capacity and loading density.

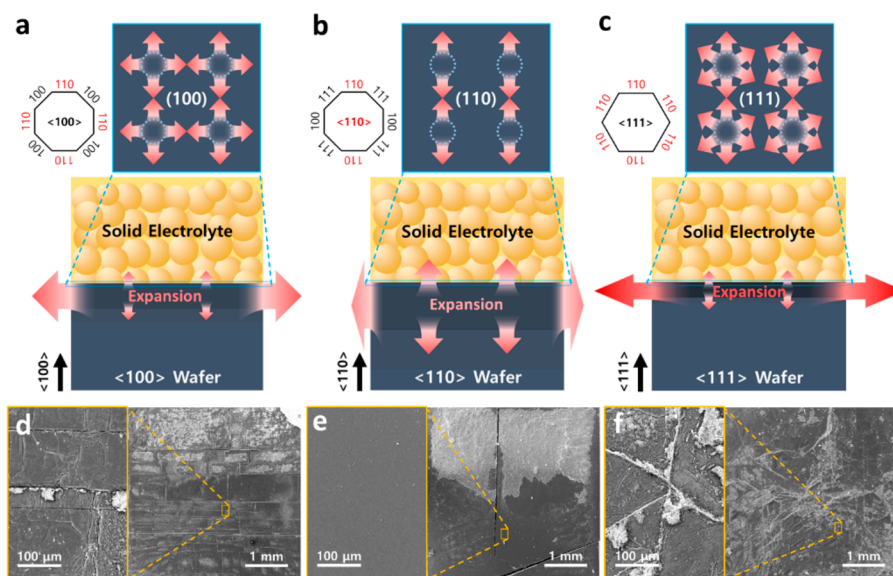
In a battery cell, the areal capacity of the electrode is one of the most important parameters in determining the electrode performance, and achieving a high areal capacity remains a big challenge in ASSBs.<sup>23–26</sup> In this study, we demonstrate that a monolithic, void-free silicon electrode can successfully reach an extremely high areal capacity of  $10 \text{ mAh cm}^{-2}$ . Thin wafers are attractive model geometries for realizing additive-free, electrolyte-free, and void-free electrodes, and are highly compatible with the microfabrication and mass-production infrastructure. Monolithic silicon wafers do not need solid electrolytes or conducting carbon additives inside and can fundamentally suppress parasitic side reactions at interfaces or SEI growth within the electrode. Moreover, monolithically integrated silicon–silicon bonding networks allow facile lithium transport through the thickness direction, utilizing the active materials deeply and enabling a high areal capacity. Specifically, it is challenging to increase the loading density to higher than  $1.5 \text{ g cm}^{-3}$  for the powder electrode. The highest reported loading amount of silicon powder in an ASSB electrode is  $1.41 \text{ g cm}^{-3}$ , achieved using 99.9% silicon powder.<sup>27</sup> Meanwhile for the silicon wafer, the loading amount is  $2.2 \text{ g cm}^{-3}$ , which is almost twice as high as that of the powder electrode (Figure S1). Silicon wafers are potentially favorable battery anodes in terms of large-scale manufacturing and commercialization due to their mature production in accordance with semiconductor or solar cell production. Furthermore, and in contrast to solid electrolyte composed silicon electrodes, silicon wafers are stable in ambient conditions, which would avoid the need for specialized facilities to maintain dry conditions during solid state anode fabrication. Several previous studies have reported the fundamental mechanisms of electrochemical lithium insertion in silicon wafers in liquid electrolyte systems.<sup>28–36</sup> However, in this study, we report on the outstanding performance of silicon wafer cells in solid electrolyte systems, achieving an increased cycle retention of up to 100 cycles by controlling the surface morphology. Additionally, we have successfully operated a full-cell with a Ni-rich NCM cathode.

Although the monolithic and void-free electrode geometry is ideal for achieving the maximum energy density, the use of a pure silicon wafer as an anode for conventional liquid electrolytes lithium-ion batteries has not been successful. The liquid electrolyte could freely penetrate the electrode through defects or cracks, create fresh SEI, and lead to pulverization because the silicon wafer repeatedly expands and shrinks upon cycling, as shown in Figure 1a.<sup>32,37,38</sup> In ASSBs, the solid electrolyte can densely form 2-dimensional interfaces with the silicon wafer surface, hold the silicon surfaces, and suppress the mechanical failure of silicon during cycling. Because a rigid solid electrolyte cannot penetrate deeply through the silicon electrode, a 2-dimensional interface between the solid electrolyte and silicon wafer could persist, and a detrimental percolated SEI within the electrode does not easily form.

Here, we present the battery performance of a bare <100> silicon wafer with 1.0 M LiPF<sub>6</sub> in ethylene carbonate (EC) and dimethyl carbonate (DMC) (1:1 v/v %) liquid electrolyte and Li<sub>6</sub>PS<sub>5</sub>Cl (LPSCl) solid electrolyte as shown in Figure 1b. It is clear that the silicon wafer lost electrical contact significantly during the first dealloying process in the liquid electrolyte (Figure S2) while it efficiently cycled 19 times in the solid electrolyte at a current density of  $0.5 \text{ mA cm}^{-2}$  under cutoff areal capacity of  $10 \text{ mAh cm}^{-2}$ . This confirms that silicon wafers have a remarkable potential as high-capacity anodes for ASSBs.

To enhance the compatibility of silicon wafers with solid electrolytes in ASSBs, we evaluated the effect of the crystallographic orientation on lithium diffusion within the electrode. Considering the diamond cubic structure with the Fd $\bar{3}$ m space group shown in Figure S3, the lattice position displayed along the <110> direction had the largest interstitial spacing and contributed to the fastest lithium diffusion in the <100>, <110>, and <111> directions.<sup>39,40</sup>

Figure 1c shows the battery performance of the bare <100>, <110>, and <111> wafers tested at a galvanostatic current density of  $0.5 \text{ mA cm}^{-2}$ . The wafers in this study were used as received from the manufacturers. The thicknesses were 200, 500, and  $350 \text{ }\mu\text{m}$  for bare <100>, <110>, and <111>, respectively. Figure S4 shows the lithiation depth of bare <110> wafers with different thicknesses of 250 and  $500 \text{ }\mu\text{m}$ .

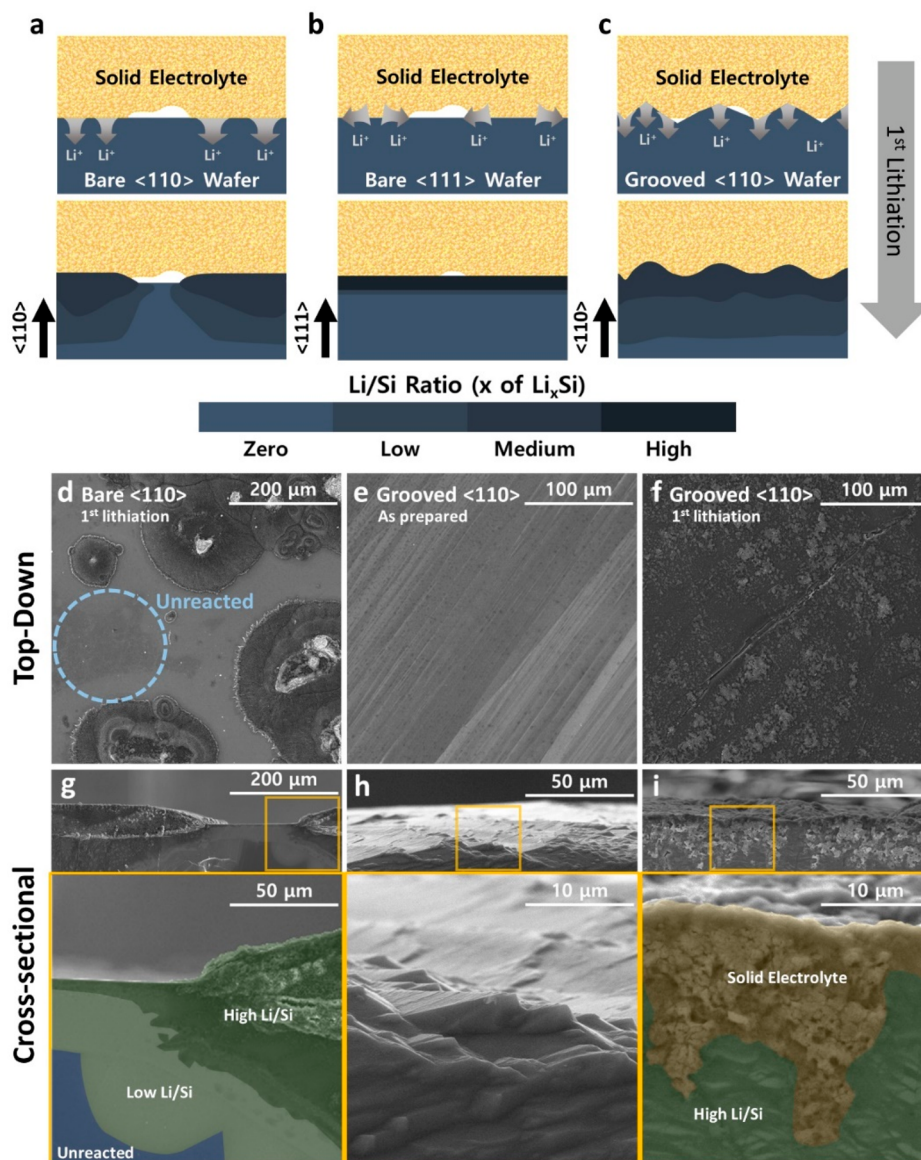


**Figure 2.** Cracks evolved along [110] direction due to anisotropic volume expansion of wafers. (a–c) Schematic of plane and side views showing major expansion directions along [110] for each wafer. (d–f) Top-down SEM images of first lithiated bare <100>, <110>, and <111> wafer surfaces.

The lithiation depth is approximately 160  $\mu\text{m}$  and constant for both wafers, which confirms that the thickness does not play a significant role in the battery performance. Also, unreacted silicon at the bottom remains unreacted and does not interfere the battery performance. They are sufficiently thick to accommodate a high areal capacity and alloyed lithium, enabling the evaluation of the intrinsic properties of lithium transport depending on the crystallographic orientation of the wafers. For instance, the cutoff lithiation areal capacity (10  $\text{mAh cm}^{-2}$ ) still leaves an unreacted silicon substrate underneath and allows cross-sectional scanning electron microscopy (SEM) to visualize the lithiated and unreacted regions by image contrast. Figure 1b–d presents the cyclability, voltage profiles, and  $dQ/dV$  profiles of each cell at current density of 0.5  $\text{mA cm}^{-2}$  under cutoff areal capacity of 10  $\text{mAh cm}^{-2}$ . The cell of the bare <110> wafer exhibited the best cyclability of 44 cycles, followed by that of the bare <100> wafer (19 cycles) and bare <111> wafer (11 cycles). The alloyed lithium amounts were constant for all, but the lithium transport depths varied with the wafer orientation. We note that the  $dQ/dV$  profile in Figure 1d during lithiation still diverges and does not have a peak, indicating that the full lithiation capacity has not been reached. The voltage end-points (inset image of Figure 1d) in bare <100>, <110>, and <111> are 0.075, 0.082, and 0.057 V, respectively, and could correlate with the effective lithium composition within the active silicon–lithium alloy regions. Figure 1e–g shows that the depths of the lithiated alloys of bare <100>, <110>, and <111> were 80, 160, and 55  $\mu\text{m}$ , respectively. The highest voltage end point for bare <110> indicates a low lithium  $\langle x \rangle$  fraction within the  $\text{Li}_x\text{Si}$  alloy and deeper lithium diffusion along the wafer thickness, as characterized by the SEM image in Figure 1f. This confirms that lithium diffuses rapidly along the <110> depth direction in the bare <110> wafer. In contrast, point A of the bare <111> wafer is the lowest, indicating the highest lithium  $\langle x \rangle$  fraction within  $\text{Li}_x\text{Si}$ , consistent with the SEM images in Figure 1g showing lithium alloys confined near the solid electrolyte interfaces.

Lithiation expands the crystalline silicon electrodes significantly along the [110] direction and only slightly along the [100] and [111] directions.<sup>39</sup> Figure 2a–c displays the preferred expansion directions for each orientation wafer; the <100>, <110>, and <111> wafers have four, two, and six in-plane [110] directions, respectively. The in-plane expansion of the silicon wafer near the interface of the bare <111> wafer was the most severe among the three, followed by the bare <100> and bare <110> wafers. The significant volume expansion along the [110] direction leads to the release of strong compressive stress after lithiation, promoting cracks along the [110] direction. The top-down SEM images of the first lithiated wafer surfaces in Figure 2d–f show the cracks generated along the [110] direction, in which rectangularly shaped cracks and triangular/hexagonally shaped cracks were generated for the bare <100> wafer and bare <111> wafer, respectively. In contrast, the bare <110> wafer allows fast lithium diffusion along the <110> thickness direction, effectively suppressing the in-plane expansion while allowing thickness-direction expansion. Thus, cracks rarely form on the electrode surface, maintaining a monolithic electrode structure upon cycling. Cross-sectional SEM images demonstrated that lithium was more evenly distributed along the thickness, releasing the stress more homogeneously within the electrode in the bare <110> wafers. In contrast, lithium is highly concentrated near the surface of the bare <111> wafer, which is consistent with the  $dQ/dV$  plot and could lead to a high local stress at the interface. Thus, the <110> orientation is the optimal choice as a crystalline wafer anode in ASSBs.

Although the <110> orientation would be more ideal than the others, homogeneously utilizing the entire electrode surface is critical and remains challenging. In practice, it may be difficult to realize a conformal interface between the solid electrolyte and flat electrode surfaces, and faster interfacial domains lead to the lithiation of the current hotspots. The interfaces that initiate lithiation at the beginning of charging expand vertically and push the solid electrolyte along the <110> direction, making the fast interface more densely contacted. However, this widens the gap between the slow and

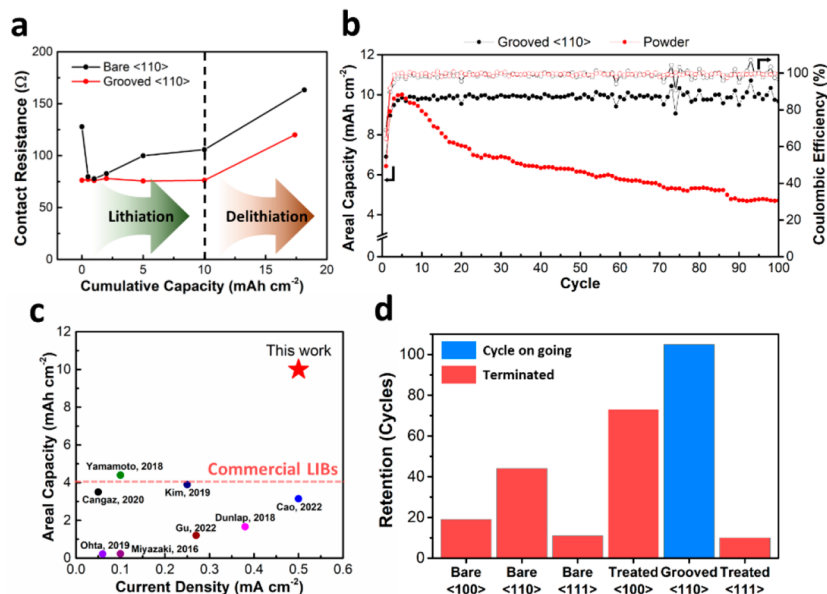


**Figure 3.** Surface treated <110> wafer. (a–c) Schematic of lithiation at uneven interfaces between solid electrolyte and wafer. (d–i) Top-down and cross-sectional SEM images of first lithiated bare <110>, pristine grooved <110>, and first lithiated grooved <110> wafers.

inactive interfaces, delaminating certain electrode surfaces from the electrolyte (Figure 3a). The SEM images shown in Figure 3d,g, and Figure S5 illustrate the unreacted area left on the bare <110> wafer surface after the first lithiation. We confirmed that the unreacted area of silicon wafers is not lithiated using time-of-flight secondary ion mass spectrometry and Raman spectroscopy as shown in Figures S6 and S7. These unreacted areas could not be found for bare <111> wafers because lithium tends to diffuse laterally (in-plane direction) along the interface, increasing the active interfacial regions (Figure 3b). Figures 1g and 2f confirm that the entire surface was active and lithiated.

To improve the contact between the electrolyte and electrode and increase electrode utilization, we etched bare <110> wafers with KOH to create a groove structure on the surface at room temperature for 24 h, which also decreased the wafer thickness (Figure 3c,e,h). We investigated and quantified the surface morphology by atomic force microscopy (AFM) and surface profiler, which showed a mild roughness increase

on the nanoscale, and a limited roughness increase on the microscale for the grooved wafers as compared to bare wafers. This is consistent with results from X-ray photoelectron spectroscopy (XPS), which show a mild increase in surface oxidation of the silicon wafer. AFM and profiler images are shown in Figures S8–S10. XPS results are shown in Figure S11 and Table S1. Additional details and procedures are explained in the Supporting Information. The grooves on the silicon surface could effectively penetrate the sulfide electrolyte layers, which have sufficient ductility under the cell fabrication pressure (~500 MPa), creating a conformal contact (Figure S12). The grooved interface effectively increased the interfacial area for facile lithiation, and silicon grooves (and corresponding crests) more intimately interface with the solid electrolyte, leading to more efficiently and homogeneously distributed lithiation current across the entire silicon wafer (Figure 3c and Figure S13). Moreover, we note that silicon grooves could strongly bind the sulfide electrolyte, and the SEM plane and side-view images of the electrode after the first lithiation show



**Figure 4.** Performance of the grooved <110> wafer. (a) Contact resistance calculated by fitting the Nyquist plots (Figure S18, Supporting Information) during the first cycle. (b) Cycling performance of the grooved <110> wafer and powder electrode. (c) Performance comparison of the grooved <110> wafer half-cell with previously reported ASSB silicon electrode half-cells.<sup>16,17,41–46</sup> (d) Cycle retentions of bare and treated <100>, <110>, and <111> wafers.

that the surfaces are entirely covered by the sulfide electrolyte after disassembling the cell (Figure 3f,i and Figure S14). After delithiation of the grooved <110> wafer cell, the grooves on the surface remained, and we could not observe any significant mechanical damage to the solid electrolyte layer, as shown in the SEM images of Figures S15 and S16. This is contrary to the bare <110> wafer, which exhibits delaminated and clean surfaces with no sulfide electrolyte after cell disassembly.

Galvanostatic cycling of the grooved <110> wafer was performed at  $0.5 \text{ mA cm}^{-2}$ . The voltage profile in Figure S17 shows a lower overpotential and remains more stable compared with that of the bare <110> wafer owing to the stable interface. We characterized the contact resistance via electrochemical impedance spectroscopy (EIS) and found that the grooved <110> wafer showed significantly lower and more consistent contact resistance during lithiation than the bare <110> wafer. The high resistance that decreases at the beginning of the cycle for the bare <110> wafer indicates that the poorly contacted interface between the electrode and electrolyte is densely packed via the depth-direction expansion of the electrode upon lithiation. The consistently low contact resistance of the grooved <110> wafer indicates that the grooved surfaces could effectively penetrate the solid electrolyte during cell fabrication and maintain the integrity of the contact interfaces during cycling (Figure 4a).

The grooved <110> wafer shows a remarkable cycle life and stably achieves an areal capacity of  $10 \text{ mAh cm}^{-2}$  at a current density of  $0.5 \text{ mA cm}^{-2}$  at room temperature (Figure 4b). The grooved wafers became significantly thinner ( $220 \mu\text{m}$ ) after KOH etching, indicating that the material cost could be further reduced. Additionally, the thinned wafer could effectively limit lithium diffusion along the thickness direction and efficiently allow lithium to be extracted reversibly during delithiation. Further thinning and optimizing the wafer thickness can extend the Coulombic efficiency and cycle life.

In contrast, achieving a high areal capacity of as much as  $10 \text{ mAh cm}^{-2}$  for the conventional silicon powder electrode is not

straightforward at room temperature. We attempted to fabricate a thick silicon powder anode and our optimized maximum loading density of the silicon powder anode was  $8.3 \text{ mg cm}^{-2}$  at best (the theoretical areal capacity is  $29.8 \text{ mA/cm}^2$ ). Our thick powder electrode demonstrated an areal capacity of  $10 \text{ mAh cm}^{-2}$  at the beginning of the cycle, which decreased to  $5 \text{ mAh cm}^{-2}$  after 100 cycles. It remains challenging for silicon powder electrodes to eliminate voids and pores under an acceptable fabrication pressure of 500 MPa. They significantly retard lithium transport and decrease the energy density. Thus, conventionally developed powder or nanoparticle-based composite electrodes mixed with solid electrolyte particles or thin-film electrodes for ASSBs show difficulty in achieving a high areal capacity of  $10 \text{ mAh cm}^{-2}$  at room temperature. To the best of our knowledge, our grooved <110> wafers showed the highest areal capacity at room temperature among the reported silicon anodes developed for ASSB half-cells. (Figure 4c).<sup>16,17,41–46</sup>

The other <100> and <111> wafers were treated with KOH. Their battery cycle lives were 73 cycles and 10 cycles, respectively, and they could not outperform the grooved <110> wafer, as expected. Figure 4d shows the cycle retention of all silicon wafers until the delithiation capacity reached  $8 \text{ mAh cm}^{-2}$ . It is widely known that KOH cannot effectively groove <111> wafers, but only considers it. We attribute the poor cycle retention of KOH-etched <111> wafers to poor lithium diffusion along the <111> direction and ineffective surface treatment.

We further demonstrated that our grooved <110> wafer is highly compatible with a Ni-rich NCM cathode and achieved an areal capacity of  $8.5\text{--}8.8 \text{ mAh cm}^{-2}$  at room temperature and  $60^\circ\text{C}$ , as shown in Figure S19. The current density and the voltage ranges are  $0.5 \text{ mA cm}^{-2}$  and  $2\text{--}4.3 \text{ V}$ , respectively. To match the high areal capacity of the anode, we attempted to develop a high-loading NCM cathode with a thickness of  $380 \mu\text{m}$ , the thick electrode being beyond the scope of this study. To stably utilize a thick cathode, we operated the full-cell at an

elevated temperature, which could run stably and report a discharge capacity of 8.8 mAh cm<sup>-2</sup>. This indicates that silicon wafers are promising anode candidates for high-areal-capacity ASSB full-cells.

In this study, we successfully demonstrated that a void-free monolithic pure silicon electrode could achieve an areal capacity as high as 10 mAh cm<sup>-2</sup> in a half-cell at room temperature and 8.8 mAh cm<sup>-2</sup> in a full-cell at 60 °C. The monolithic silicon structure allowed fast lithium transport across the electrode thickness, and surface modification enhanced the interfacial stability and cycle retention. Our results clearly showed that silicon wafers, which have been largely overlooked in liquid-electrolyte batteries, have great potential as next-generation electrodes for ASSBs. Combined with modern microfabrication technologies, the surface, thickness, crystallinity, and defects, etc. can be sophisticatedly engineered to deliver a superior energy density, rate capability, and cycle-life. Specifically, silicon wafers can be precisely and systematically micropatterned and etched to optimize the unit size of monolithic silicon geometry and their distance from each other. Such geometry can minimize dilation upon expansion and allow the solid electrolyte to be effectively percolated for a fast lithium pathway and long cycle life. In addition, our results on monolithic Si anodes open a new avenue for next-generation high-energy ASSBs.

## ■ ASSOCIATED CONTENT

### SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsenerylett.3c00496>.

Experimental methods; atomic force microscopy (AFM) analysis; X-ray photoelectron spectroscopy (XPS) analysis; silicon density measurements; a voltage profile of a silicon wafer under the liquid electrolyte system; a plot of lithium diffusivity in the crystalline silicon; SEM and optical microscopy images of the lithiated and delithiated wafers and solid electrolyte; 2D mapping images of time-of-flight secondary ion mass spectrometry (ToF-SIMS); Raman spectroscopy results; surface profiler results; Nyquist plots of the wafers; energy dispersive X-ray spectroscopy (EDS) maps of the first lithiated wafer (PDF)

## ■ AUTHOR INFORMATION

### Corresponding Author

**Jongwoo Lim** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea; [orcid.org/0000-0002-3897-7488](https://orcid.org/0000-0002-3897-7488); Email: [jwlim@snu.ac.kr](mailto:jwlim@snu.ac.kr)

### Authors

**Ikcheon Na** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea  
**Hwiho Kim** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea  
**Sebastian Kunze** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea  
**Chihyun Nam** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea  
**Sugeun Jo** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea  
**Hanbi Choi** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea

**Sumin Oh** – Department of Chemistry, Seoul National University, 08826 Seoul, South Korea

**Eugene Choi** – Department of Mechanical Engineering, Seoul National University, 08826 Seoul, South Korea

**Yong Bae Song** – Department of Chemistry and Biomolecular Engineering, Yonsei University, 03722 Seoul, South Korea

**Yoon Seok Jung** – Department of Chemistry and Biomolecular Engineering, Yonsei University, 03722 Seoul, South Korea; [orcid.org/0000-0003-0357-9508](https://orcid.org/0000-0003-0357-9508)

**Yun Seog Lee** – Department of Mechanical Engineering, Seoul National University, 08826 Seoul, South Korea; [orcid.org/0000-0002-2289-109X](https://orcid.org/0000-0002-2289-109X)

Complete contact information is available at:

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## Notes

The authors declare no competing financial interest.

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